

AMENDMENTS TO THE SPECIFICATION

Please substitute the following amended paragraph [0014] with the currently pending paragraph [0014].

[0014] In one embodiment of the present invention, IC 100 is a field programmable gate array that further contains a plurality of input-output (I/O) blocks, such as blocks 122-125, and a plurality of configurable logic blocks (CLBs) which provide functional elements for constructing logic, such as blocks 127-128. Detail description of these blocks can be found in "The Programmable Logic Data Book 2000," Chapter 3, published by Xilinx, Inc, the content of which is incorporated herein by reference. These blocks can be used to build other circuits that may be connected to the system of the present invention. The circuit of Fig. 1 also provides a programmable routing matrix 129. The programmable routing matrix could provide local routing, general purpose routing, I/O routing or dedicated routing. For example, local routing resources could comprise interconnections among CLBs and routing matrices, internal CLB feedback paths that provide high-speed connections to look-up tables within the same CLB, or direct paths that provide high-speed connections between horizontally adjacent CLBs. General purpose routing could comprise a routing matrix having routing resources located in horizontal and vertical routing channels associated with the CLB rows and columns. The programmable routing matrix could also comprise additional routing resources that form an interface between CLBs and the IOBs. Finally, some classes of signals require dedicated routing resources to maximize performance.